AMENDMENTS TO THE CLAIMS

1.   (Currently Amended):   A data output circuit which outputs data on ~~an~~ internal bus line<u>s</u> onto ~~an~~ external bus line<u>s</u>, comprising:

comparison means for comparing data on<u> groups of</u> the external bus line<u>s</u> and data ~~to be output~~ on <u>corresponding groups of</u> the internal bus line<u>s</u>;

inversion means for outputting ~~a signal~~ <u>inverted data</u> obtained by inverting the data on ~~the~~ <u>a respective group of</u> internal bus line<u>s</u> when the number of changed bits exceeds half the total number of bits <u>in that group</u> on the basis of an output result from said comparison means; and

control means for outputting an inversion display signal representing that the data <u>in a particular group</u> has been inverted.

2.   (Original):   A circuit according to claim 1, wherein said comparison means, said inversion means, and said control means constitute an output data control unit.

3.   (Original):   A circuit according to claim 2, further comprising:
an amplifier which amplifies read data;
data latch means for latching data output from said amplifier; and
input/output means for transmitting an output data bus signal from said output data control unit as output data onto the external data bus.

4.   (Original):   A circuit according to claim 3, wherein said input/output means feeds back the output data to said comparison means.

5.   (Original):   A circuit according to claim 3, further comprising clock signal supply means for supplying a clock signal to said data latch means, said output data control unit, and said input/output means.

6.   (Currently Amended):   A circuit according to claim 1, wherein the data on the internal bus ~~line~~ <u>lines</u> includes data read out from storage means.

7.   (canceled)

8.   (Currently Amended):   A data output method of outputting data on ~~an~~ internal bus line<u>s</u> onto ~~an~~ external bus line<u>s</u>, comprising the steps of:

<u>arranging each of the internal and external bus lines into a plurality of corresponding groups,</u>

comparing data on ~~the external bus line and data to be output on the~~ <u>each</u> <u>group of</u> the internal bus line<u>s</u> <u>to data on corresponding groups of external bus lines</u>;

when the number of changed bits <u>in a particular group</u> exceeds half <u>of</u> the total number of bits <u>in that group,</u> on the basis of a comparison result, inverting the data on the <u>particular group of</u> internal bus line<u>s</u> to output the data onto the <u>corresponding group of</u> external bus line<u>s</u>; and

outputting a data inversion signal representing that the data <u>in the particular group</u> has been inverted.

9.   (Original):   A method according to claim 8, wherein the comparison step comprises the step of receiving a clock signal.

10.   (Original):   A method according to claim 8, further comprising the step of reading out the data on the internal bus line from storage means.

11.   (Canceled)